THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 72

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DOUGLAS PELTZER

Appeal No. 95-2454
Application No. 07/396,733[1]

ON BRIEF

Before KIMLIN, SCHAFER and WEIFFENBACH, Administrative Patent Judges.
SCHAFER, Administrative Patent Judge.

DECISION UNDER 35 U.S.C. § 134

BACKGROUND

The subject matter of this appeal generally relates a method for making integrated circuit devices. Specification, p. 1, lines 1-3. Integrated circuits are electrical circuits having the individual units or components of the circuit formed in or on a semi-conductor material such as silicon. These components

[1] Application for patent filed August 18, 1989. According to appellant, this application is a continuation of application 05/187,124, filed October 6, 1971, now abandoned; which is a division of U.S. Patent 3,648,125, based upon application 05/111,956, filed February 2, 1971.

include transistors, diodes, resistors, etc. which are interconnected to form the desired circuit. In order for the circuit to perform its function, the various components must be electrically isolated from each other (except of course for the necessary conductive pathways which join the individual elements into the circuit). The active and passive circuit elements of the circuit are formed within these electrically isolated regions or pockets. Various techniques have been used for achieving the necessary isolation. Specification, p. 1, lines 4-6. In the integrated circuits made by applicant's method, electrical isolation between regions is achieved by the combination of an underlying PN junction and channels of silicon dioxide which contacts the PN junction. This structure can be seen from the much simplified and annotated version of applicant's Figure 4:

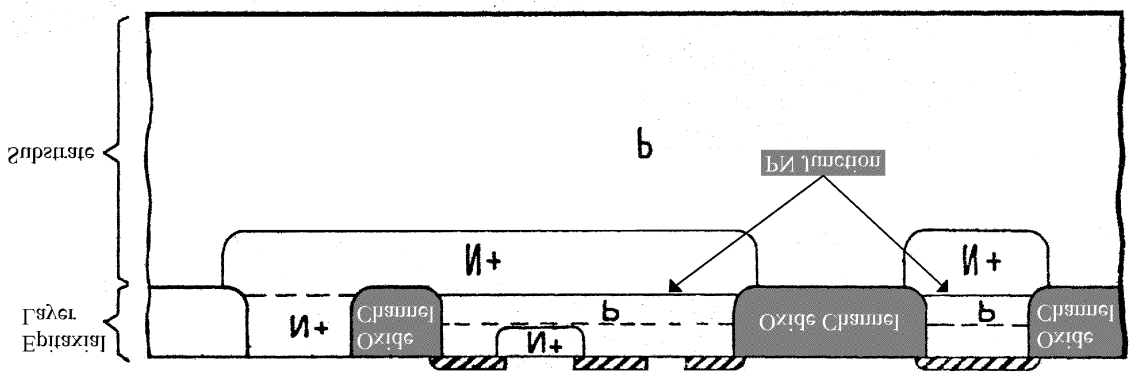

FIG. 4

Applicant's process begins with a doped silicon substrate. In the first part of the process, a PN junction is formed. This is done by growing an epitaxial silicon layer on at least a portion of the substrate to form a PN junction. Depending on the type of component desired, the epitaxial layer may be

the same or opposite conductivity type as the substrate. In the case of the latter, a PN junction is directly formed at the interface of the substrate and the epitaxial layer. In the case of the former, a region of the opposite conductivity type is first formed in the substrate and then the epitaxial layer of the same conductivity type as the substrate is grown on the substrate forming the PN junction. In the next part of applicant's process the insulating channels are formed. A layer of insulation is placed over the epitaxial layer. The layer may be silicon nitride or any material which is unaffected by silicon etchants and masks against thermal oxidation of the underlying semiconductor material. The portions of the insulation over areas of the epitaxial layer to be oxidized are removed. A portion of the exposed epitaxial silicon is then removed by etching to form channels. The exposed silicon is oxidized. The amount of epitaxial silicon removed is controlled so that upon oxidation (1) the oxide layer reaches the PN junction and (2) fills the grooves with oxide so that the surface of the oxide layer is substantially coplanar with the original surface of the epitaxial layer. The oxide channels, along with the underlying PN junction, form electrically isolated regions of semi-conductor material.

Applicant's independent claims 14 and 25 are representative and are reproduced in the margin.[2]

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[2] 14. The method of forming a plurality of electrically isolated pockets of semiconductor material in a semiconductor structure comprising a silicon substrate of one conductivity type with an epitaxial silicon layer of opposite conductivity type thereon, which comprises the steps of:

growing a doped epitaxial silicon layer on said silicon substrate, said doped epitaxial silicon layer having a conductivity type relative to the conductivity type of at least a, portion of the top surface of said substrate such that a laterally-extending PN junction is formed in at least part of said semiconductor structure;

forming a layer of insulation on said epitaxial silicon layer, said insulation having the properties that it is substantially unaffected by at least one etchant used to remove epitaxial silicon and substantially masks the diffusion of oxygen;

removing portions of said insulation overlying regions of said epitaxial silicon layer to be converted into oxidized silicon;

forming depressions to a specified depth in said epitaxial silicon exposed by removal of said insulation by removing part of said epitaxial silicon exposed by removal of said insulation; and

subdividing said epitaxial silicon layer into a plurality of electrically isolated pockets of semiconductor material by oxidizing the silicon exposed by said depressions to form oxidized silicon extending through said epitaxial silicon layer to said PN junction;

(continued...)

Forming electrically isolated regions during the production of integrated circuits is not new in the art. Applicant notes in the specification that electrical isolation has been achieved by surrounding the region to be isolated with PN junctions. This structure is illustrated by the simplified and annotated version of applicant's Figure 1 below. In the figure the surrounding PN-junction is formed by the P+ isolation "channels" or regions and the underlying PN junction.

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[2](...continued)

wherein the depth and shape of said depressions is selected such that the oxidized silicon has an upper surface substantially coplanar with the top surface of said epitaxial silicon layer and a bottom surface which extends through said epitaxial silicon layer to said PN junction, thereby both to surround each pocket by an annular-shaped region of oxidized silicon and to electrically isolate each pocket by an annular-shaped region of oxidized silicon and a portion of said laterally-extending PN junction.

25. The method of forming a plurality of electrically isolated pockets of semiconductor material in a semiconductor structure comprising a silicon substrate of one conductivity type with an epitaxial silicon layer thereon of said one conductivity type which comprises the steps of:

forming directly beneath portions of the top surface of said substrate low resistivity regions of opposite conductivity type to said one conductivity type, such that a laterally-extending PN junction is formed between said low resistivity regions and said silicon substrate;

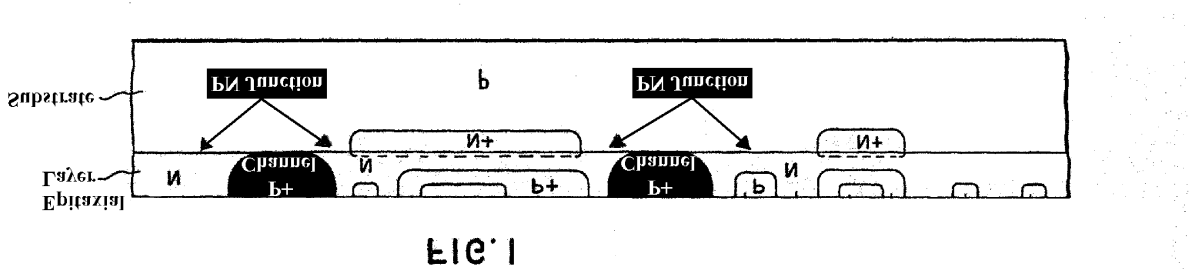
growing a doped epitaxial silicon layer of said one conductivity type on said silicon substrate;

forming a layer of insulation on the top surface of said epitaxial silicon layer, said insulation having the properties that it is substantially unaffected by at least one etchant used to remove epitaxial silicon and substantially masks the diffusion of oxygen;

removing portions of said insulation overlying regions of said ~epitaxial silicon layer to be converted into oxidized silicon;

forming depressions to a specified depth in said ~epitaxial silicon exposed by removal of said insulation by removing part of said epitaxial silicon exposed by removal of said insulation; and subdividing said ~epitaxial silicon layer into a plurality of electrically isolated pockets of semiconductor material by oxidizing the silicon exposed by said depressions to form oxidized silicon;

wherein said depth is selected such that the oxidized silicon has an upper surface approximately coplanar with the top surface of the remaining portions of said epitaxial layer and has a bottom surface in contact with said laterally extending PN junction thereby to surround each pocket of semiconductor material by an annular-shaped region of oxidized silicon.



The P+ isolation regions are formed by diffusion of an appropriate impurity into the epitaxial layer. Specification, pp. 6-8.

The rejections

The examiner presents four separate grounds of rejection:

1. The subject matter of claims 2, 3, 5-9, 12, 14, 15, 19, 20, and 36-48 stands rejected under 35 U.S.C. § 103 over the combination of Frouin,[3] Murphy[4] and Doo;[5]

2. The subject matter of claims 25-35 and 49-59 stands rejected under 35 U.S.C. § 103 over the combination of Frouin, Murphy, and Doo and Makimoto;[6]

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[3] Frouin et al., U.S. Patent 3,500,139, issued March 10, 1970, based upon application 04/713,662, filed March 18, 1968.

[4] Murphy, U.S. Patent 3,649,386, issued March 14, 1972, based upon application 04/723,529 filed, April 23, 1968.

[5] Doo, U.S. Patent 3,386,865, issued June 4, 1968, based upon application 04/454,374, filed May 10, 1965.

[6] Makimoto, U.S. Patent 3,596,149, issued July 27, 1972, based upon application 05/4,468 filed, January 19, 1970.

3. The subject matter of claims 2, 3, 5-9, 12, 14, 15, 19, 20, and 36-48 stands rejected under 35 U.S.C. § 103 over the combination of Doo, Jones,[7] Clevenger[8] and Murphy.

4. The subject matter of claims 25-35 and 49-59 stands rejected under 35 U.S.C. § 103 over the combination of Doo, Jones, Clevenger, Murphy, Karcher[9] and Makimoto.

DECISION

We affirm the rejection of claims 2, 3, 5, 6, 12, 14, 15, 19, 20, and 25-28, 30, 36-41 and 48 over the combination of Frouin, Murphy and Doo. We reverse the rejection of claims 7-9, 42-47 and 53-58 over the combination of Frouin, Murphy and Doo. We affirm the rejection of 25-35 and 49-52 and 59 over the combination of Frouin, Murphy, and Doo and Makimoto. We reverse the rejection of claims 57 and 58 over the combination of Frouin, Murphy, and Doo and Makimoto. We reverse the rejection of claims 2, 3, 5-9, 12, 14, 19, 20, and 36-48 over the combination of Doo, Jones, Clevenger and Murphy. We reverse the rejection of claims 25-35 and 49-59 Doo, Jones, Clevenger, Murphy, Karcher and Makimoto.

ANALYSIS

The rejections based on the Frouin patent

Independent claims 14 and 36

The examiner rejects these claims over the combined teachings of Frouin, Murphy and Doo. We affirm this rejection.

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[7] Jones, "A Composite Insulator-Junction Isolation," 5 Electrochemical Technology 308 (May-June 1967).

[8] Clevenger, U.S. Patent 3,534,234, issued October 13, 1970, based upon application 04/601,970, filed December 15, 1966.

[9] Karcher, U.S. Patent 3,404,450, issued October 8, 1968, based upon application 04/523,099, filed January 26, 1966.

The Frouin patent relates to integrated circuits having regions electrically isolated by means of filled channels and a PN junction. Frouin, col. 1, lines 25-30. Frouin notes that electrical isolation of the type disclosed in applicant's Figure 1 has many drawbacks. Frouin, col. 1, lines 31-46. Frouin's solution was to form channels in the epitaxial layer which included insulating material. The channels extend from the free surface layer and intersect the PN junction. Frouin, col. 2, lines 4-9. Frouin's channels include a layer of silicon oxide on the surface and the remainder of the channel is filled with a polycrystalline semiconductor material. This structure is clearly shown in the semiconductor device shown in Frouin's Figure 1. A simplified and annotated version of Frouin's Figure 1 is reproduced below.

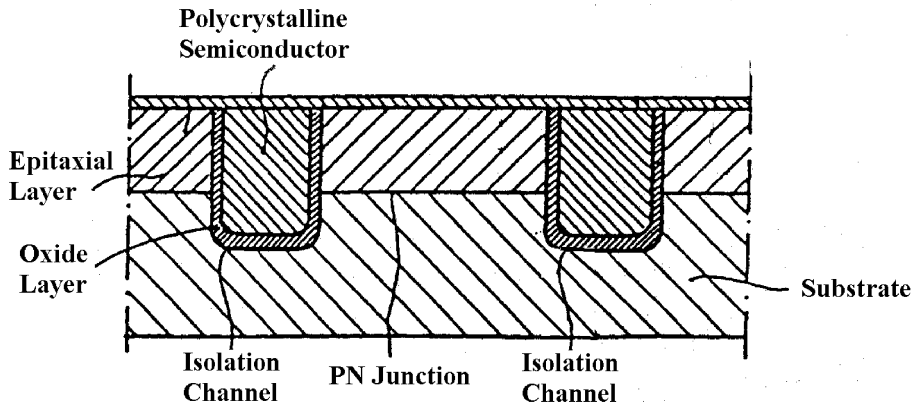

fig.1

The device includes a substrate, an epitaxial layer of a conductivity type which differs from the substrate's type, and isolation channels extending into the substrate past the PN junction. The grooves divide the device into isolated islands or pockets. The grooves include an insulating surface oxide layer and are filled with polycrystalline semiconductor material. The top of the grooves are essentially coplanar with the upper surface of the epitaxial layer. Frouin, col. 3, lines 1-10. The insulating surface layer may be silicon oxide and the polycrystalline semiconductor may be poly crystalline silicon. Frouin, col. 3, lines 57-61. The

silicon oxide layer provides the electrical insulation while the polycrystalline semiconductor merely serves as a filler. Frouin, col. 2, lines 26-30. Frouin's regions between the channels (actually surrounded by the channels) are electrically isolated by the PN junction and oxide layer on the channel surface. Frouin, col. 4, lines 7-9. One of the advantages of Frouin's design is the reduction in the size of the "dead zone," the required distance of separation of the various the components from the insulation channels. Frouin, col. 2, lines 46-50.

Frouin also describes a process for manufacturing integrated circuits having filled isolation channels. E.g., Frouin, col. 5, line 30 - col. 6, line 17. Frouin's process begins with a silicon substrate. An epitaxial layer of opposite conductivity-type is deposited on the substrate surface forming a PN junction. Frouin, col. 5, lines 30-35. Next the grooves are formed using etching and a photoresist technique. Frouin, col 5, lines 39-40. Etching using a photoresist technique includes using a layer which is substantially unaffected by at least one etchant used to remove the epitaxial silicon.[10] The resulting grooves are then coated with an insulating material such as silicon dioxide "for which process a conventional technique can be used." Frouin, col. 5, lines 41-44. Frouin also indicates that a silicon oxide layer can be applied by oxidation of the silicon. Frouin, col. 5, lines 62-63. Polycrystalline silicon is next deposited to fill the grooves. The deposition process not only fills the grooves but deposits a layer over the entire device. Frouin, col. 5, lines 44-55 and Figure 8c. The layer of polycrystalline silicon is then removed by grinding to obtain a flat surface. Frouin, col. 5, lines 56-57. This prepares the device for further processing and formation of active and passive circuit devices. Frouin, col. 5, lines 57 - col. 6, line 17. Frouin also notes that "the present

[10] While not expressly disclosed by Frouin, the photoresist technique used in conjunction with etching was well known to those working in the art at the time of applicant's invention. It involves placing a layer of light sensitive "photo-resist material" on to the substrate, exposing the layer to light having a pattern corresponding to the areas which are to be protected, developing the resist to harden the exposed areas, and stripping the unhardened areas to expose the areas to be etched. The mask of hardened photoresist is substantially unaffected by the etchant and thus allows for selective etching in forming the grooves. The hardened photoresist is then stripped.

invention is not confined to substrates of silicon, to insulation by an SiO_2-layer and to the filling of the insulating grooves by polycrystalline silicon." Frouin, col. 6, lines 48-51.

The difference between the process set out in applicant's claims 14 and 36 and the process disclosed by Frouin resides in applicant's use of a combined etchant and oxidation resistant coating, etching partially through the epitaxial layer to form a channel and oxidizing the channel to completely fill the depressions with silicon oxide rather than using a filler.

Murphy also relates to integrated circuits having electrically isolated regions. In particular, Murphy relates to a technique for filling depressions in epitaxial silicon layers by oxidation. Murphy, col. 1, lines 27-30. Murphy teaches

> the use of a multirole mask on a semiconductor surface. In one step the mask protects a portion of the semiconductor surface while the unmasked portions are partially etched away. In another step the same mask prevents oxidation of the protected portion of the semiconductor surface while the previously etched portions are oxidized. Subsequently the mask is removed in a solution which does not attack the oxide or the semiconductor surface.

Murphy, col. 2, lines 53-61. Thus, Murphy teaches the use of a single mask to both etch the desired regions in the epitaxial layer and to form the oxide insulation. Silicon nitride is taught as a suitable mask material having the characteristics of being unaffected during the etching of the epitaxial silicon and masks the diffusion of oxygen during the oxidation step. Murphy, col. 2, line 68 - col. 3, line 8; col. 3, lines 41-46. Murphy discloses that during the oxidation step approximately 440 angstroms of silicon is consumed for every 1000 angstroms of silicon oxide formed. Murphy, col. 2, lines 62-65. Murphy teaches that the epitaxial layer is etched to a predetermined depth so that during oxidation (1) the oxide extends through the epitaxial layer and (2) the depression is filled with oxide restoring a substantially planar surface to the device. Murphy, col. 3, lines 15-21.

Doo relates to integrated circuits electrically isolated by oxide channels. Doo, col. 1, lines 10-26. The oxide filled channels are depicted in Doo's Figures 1 and 6 (element 6). The oxide is preferably silicon

dioxide. Doo, col. 2, lines 30-32. Doo teaches that channels partially filled with silicon dioxide with the remainder a high temperature material such as polycrystalline silicon will also act as an insulator. Doo, col. 5, lines 12-15.

The person having ordinary skill in the art would have recognized that the incorporation of Murphy's depression filling technique into Frouin's process would eliminate (1) the need to fill the depressions with polycrystalline silicon material and (2) the subsequent grinding to remove the polycrystalline silicon material from the surface while still providing the necessary insulation. The person having ordinary skill in the art would have had a reasonable expectation that silicon oxide alone could be substituted for polycrystalline silicon and silicon oxide layer in light of Doo's teaching that silicon oxide and a combination of silicon oxide and polycrystalline silicon are interchangeable for the purpose of electrical isolation. Doo, col. 5, lines 12-16. Accordingly, we conclude that the subject matter of claims 14 and 36 would have been prima facie obvious.

Applicant argues that it would not be commercially practical to apply Murphy's teaching relating to the filling depressions with oxide to the process described by Frouin. Brief, p. 12-14. The basis for this assertion is that Murphy relates to a thin epitaxial layer of the order of 1 micron and Frouin relates to an epitaxial layer of about 10 microns. Brief, pp. 12-13. Applicant asserts that "it is extremely unlikely that it would be commercially feasible to grow a thermal recessed oxide to a thickness in the vicinity of 10 microns." Brief, p. 12.

In our view, the argument relating to commercial feasibility is not relevant to the obviousness issue before us. First, nothing in applicant's claims limits the claims to (1) any particular thickness of the epitaxial layer or (2) to a commercially feasible process. Second, as noted by the Federal Circuit:

> That a given combination would not be made by businessmen for economic reasons does not mean that persons skilled in the art would not make the combination because of some technological incompatibility. Only the latter fact would be relevant.

In re Farrenkopf, 713 F.2d 714, 718, 219 USPQ 1, 4 (Fed. Cir. 1983) citing Orthopedic Equipment Co. v. United States, 702 F.2d 1005, 1013, 217 USPQ 193, 200 (Fed. Cir. 1983). Thus, the question is one of technical rather than commercial feasibility. Applicant has not provided any evidence which shows that those having ordinary skill in the art would have recognized a technological incompatibility. Nor has applicant directed us to any evidence which supports the argument that "it is extremely unlikely that it would be commercially feasible to grow a thermal recessed oxide to a thickness in the vicinity of 10 microns." Argument of counsel on appeal cannot substitute for evidence. Weinar v. Rollform Inc., 744 F.2d 797, 806, 223 USPQ 369, 374 (Fed. Cir. 1984); Knorr v. Pearson, 671 F.2d 1368, 1373, 213 USPQ 196, 200 (CCPA 1982) ; In re Greenfield, 571 F.2d 1185, 1189, 197 USPQ 227, 230 (CCPA 1978); In re Langer, 503 F.2d 1380, 1395, 183 USPQ 288, 299 (CCPA 1974).

In any event, we find that the person having ordinary skill in the art would not interpret Frouin's teachings as being limited to epitaxial layers of at least 10 microns. While Frouin's specific examples describe an epitaxial layer of 10 microns, it is axiomatic that a reference must be considered in its entirety, and it is well established that the disclosure of a reference is not limited to specific working examples contained therein. In re Fracalossi, 681 F.2d 792, 794 n.1, 215 USPQ 569, 570 n.1 (CCPA 1982); In re Lamberti, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976). Nothing in Frouin indicates that thickness of the epitaxial or other layers is of significance in obtaining an operative integrated circuit device. The other references of record clearly teach that those working in the integrated circuit art were aware of the manufacturing techniques using thin epitaxial layers. For example, Murphy teaches the use of a one micron thick epitaxial layer is conventional in the art. Murphy, col. 5, lines 2-7. In addition, we find that the person having ordinary skill in the art would have recognized the reasonable limits of the Murphy's depression filling procedure. Murphy teaches that 440 angstroms (.44 microns) of silicon is consumed for every 1000 angstroms (1 micron) of silicon oxide formed. See, Murphy, col. 2, lines 62-65. This gives

reasonable guidance to those working in the art of the depth of the oxide filled grooves that may reasonably be used.

Applicant also argues that the examiner has improperly used applicant's claims as a road map for combining the references using impermissible hindsight. Brief p. 14-17. We disagree.

In one sense every obviousness rejection is based on hindsight. An examination of an invention for patentability cannot take place without first knowing what the invention is and then looking for the relevant prior art with knowledge of the claimed invention. Thus, merely asserting that a rejection uses hindsight reasoning is not helpful to deciding the obviousness issue. As noted by the CCPA:

> Any judgement on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper.

In re McLaughlin, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971). The information used in rejecting the claimed subject matter is disclosed in the prior art and is, therefore, within the level of ordinary skill in the art. The rejection was not based on information gleaned only from applicant's disclosure. In our view, impermissible hindsight was not used in rejecting the claimed subject matter.

Applicant notes that independent claims 14 and 36 each require 5 steps:

> (1) growing an epi layer on a silicon substrate of opposite conductivity type to the epi to form a laterally extending PN isolation junction, (2) forming an oxygen - impervious insulation layer on the epi, (3) creating one or more openings through the insulation layer, (4) removing exposed epi silicon to form one or more depressions extending partway through the epi, and (5) thermally oxidizing silicon exposed through each depression to form an isolation region of oxidized silicon that extends down to the PN junction so as to divide the epi into a plurality of

> semiconductor pockets electrically isolated from one another by the oxidized silicon and the PN isolation junction.[11]

Brief, p. 14-15. Applicant asserts that only this first step is taught by Frouin. We find Frouin to be significantly more informing to the person having ordinary skill in the art. In addition to step (1), Frouin at least implicitly teaches (2) forming an etch resistant coating (photo resist) or "insulation layer" on the epitaxial silicon layer, (3) creating openings over the areas where the silicon is to be removed, (4) etching the exposed silicon to form channels having a specified depth in the epitaxial silicon layer, and (5) thermally oxidizing the channels to form an isolation region dividing the epitaxial layer into a plurality of semiconductor pockets electrically isolated from one another by the oxidized silicon and PN isolation junction. Steps (2) to (5) are at least implicit in Frouin's disclosure at col. 5, lines 38-44:

> The grooves are formed by etching in a usual manner, using a photo-resist technique. The grooves separate the islands from one another. After forming the grooves, their walls are coated with an insulating layer 12, which in the present example preferably consists of silicon oxide, for which process a conventional technique can be used.

Etching using "a photo-resist technique" describes a process that was well known to those working in the art at the time the invention was made to include applying the photoresist coating, creating openings in the layer over the areas where the silicon is to be removed, and etching the exposed silicon. Frouin discloses that thermal oxidation is disclosed as one technique of forming a silicon oxide layer. Frouin, col. 5, lines 62-63. Thus, the difference between Frouin's disclosure and the claimed invention resides in the use of a combined etch and oxidation resistant coating, etching partially through the epitaxial layer and oxidizing the depression to completely fill the depressions with silicon oxide.

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[11] We note that applicant's characterization of the steps is not entirely accurate. The claim step corresponding to step (2) above also requires that the insulation be unaffected by the etchant used to form the depressions.

Applicant also argues to the effect that one having ordinary skill in the art would not substitute silicon oxide for polycrystalline silicon. Brief, pp. 17-19. Applicant notes that Frouin teaches that the polycrystalline silicon was chosen for use in filling the grooves because the coefficient of expansion of the polycrystalline material is substantially equal to that of the pockets. Brief, p. 18. Applicant then asserts that expansion coefficient of silicon dioxide is significantly different from the thermal expansion coefficient of silicon.

This argument is not persuasive. Applicant's unsupported assertion is contradicted by Doo's disclosure of the interchangeability of the combination of silicon oxide and polycrystalline silicon and silicon oxide alone for use in electrical isolation of integrated circuit components. Doo, col. 5, lines 12-16. Additionally, applicant has not pointed us to any evidence in the record supporting the assertion that the expansion coefficients of silicon oxide and silicon are "significantly different." Counsel argument can not take the place of evidence in the record. Weinar., 744 F.2d at 806, 223 USPQ at 374; Knorr, 671 F.2d at 1373, 213 USPQ at 200; Greenfield, 571 F.2d at 1189, 197 USPQ at 230; Langer, 503 F.2d at 1395, 183 USPQ at 299.

Applicant asserts that there are a number of additional considerations that show the claimed subject matter is patentable. Brief, pp. 34-38. Applicant argues (1) that the claimed method is widely used by other companies, (2) that the industry has recognized the method as a major advancement in the art, and (3) that the claimed invention satisfied a long felt need and has achieved commercial success. Applicant's rely on Exhibits C9-C15 as being evidence of third-party usage of the invention. We do not agree. Applicant has failed to provide evidence sufficient to prove these points.

Exhibits C9-C15 are copies of publications or patents. Applicant has not identified the portions of these documents where each limitation of the claimed process is described or where in the document it indicates that any processes therein described have actually been used for wide scale commercial manufacture of integrated circuits. Applicant has merely directed this board's attention to a number of

documents. In our view, it is not asking too much of an appellant to identify in the brief the specific portions of the evidence supporting appellant's argument. See, Clintec Nutrition Co. v. Baxa Corp., 44 USPQ2d 1719, 1723 n.16 (N.D. Ill. 1997). We decline to venture into this type of analysis without guidance from the applicant. We also note that a mere description of a process in a publication or patent may indicate that others knew of the process, but does not, standing alone, indicate that the process is in commercial use by the authors of the publication or others.

Applicant also argues that the claimed invention has been recognized in the industry as a major advancement. Brief, p. 35. It is asserted that the claimed subject matter is referred to in the industry as the "isoplanar process." Applicant then refers to documents allegedly indicating that integrated circuit manufacturers found the isoplanar technique as a significant development.

Again applicant has not identified the specific portions of the evidence showing that the claimed process as specifically set out in applicant's claims is commonly referred to as the isoplanar process. Indeed, it appears that the process described by Frouin and Murphy could also be referred to as an "isoplanar process." Each of these references teaches a process in which the oxide isolation channel is substantially coplanar with the top surface of the epitaxial layer. See Frouin, Figure 8c and Murphy, Figure 5.

Applicant also argues that the invention has been recognized in the "patent business." Applicant notes that U.S. patent 3,648,125, said to be directed to the integrated circuits made by the claimed method, has been cited in over 100 subsequently issued patents. Brief, p. 35. We see no persuasive value in the fact that the invention has received "recognition" in the "patent business." Recognition in the patent business, in our view, is simply not relevant to the obviousness issue. Obviousness is determined from the perspective of the hypothetical person having ordinary skill in the art --a hypothetical worker in the art-- not from the perspective of someone in the patent business. In any event, we fail to see how the mere fact that a patent has been often cited during the prosecution relating to other inventions proves the importance

of the invention. Patents are cited in applications for many purposes. In order to give the fact of numerous citations any weight it would be necessary to prove the reasons why the patent was cited. We have not been directed to any such evidence.

In summary, applicant has failed to prove that the specific subject matter of the claims is used for "wide-scale commercial IC fabrication" or has achieved wide scale industry recognition as a major advance in the art.

Applicant has also asserted that

> the present invention has been, and continues to be, a huge commercial success. The invention has fulfilled the long-felt need of increasing IC packing density and has received considerable industry recognition for being able to do so.

Brief, p. 36. As evidence of commercial success, generally relies upon the same publications and patents relied upon for showing acceptance in the industry. However, we have not been directed to evidence of market share, growth in market share, or replacing earlier units sold by others or of dollar amounts which are indicia of commercial success. Kansas Jack, Inc. v. Kuhn, 719 F.2d 1144, 1151, 219 USPQ 857, 861 (Fed. Cir. 1983). Nor have we been directed to evidence of a nexus between the alleged successful commercialization and the merits of the invention. As we indicated above applicant has not even pointed out where in the evidence, the specific limitations of the claims are disclosed. Prima facie evidence of a nexus requires that the purported commercial success flow from the invention as claimed.

As to applicant's assertion that the claimed invention satisfied a long felt need, again the evidence falls short. To show long felt need requires evidence that a problem existed in the art without solution, i.e., that others had tried and failed to find a solution. In re Mixon, 470 F.2d 1374, 1377, 176 USPQ 296, 299 (CCPA 1973); In re Allen, 324 F.2d 993, 997, 139 USPQ 492, 495 (CCPA 1963). Applicant has not directed us to evidence which shows that others had tried and failed to solve the problem. Applicant asserts that the long felt need satisfied by the invention was increased integrated circuit packing density.

Brief, p. 36. However, this problem had already been solved in the art, for example, by Frouin's technique which appears to solve the same problem. Frouin expressly teaches that

> it is possible considerably to reduce the peripheral zone referred to as the "dead region," which is usually formed around each integrated circuit unit and above which the contacts for external connections are present.

Frouin, col. 2, lines 46-50.

Claims 25 and 49

Independent claims 25 and 49 require that the epitaxial layer and the substrate be of the same conductivity type and require the additional step of forming a region of opposite conductivity type in the substrate prior to the growth of the epitaxial layer. The examiner relies on Makimoto in addition to Frouin, Murphy and Doo in rejecting these claims.

Makimoto discloses forming regions in the substrate having a conductivity type which is opposite to that of the substrate and covering the substrate and the regions with an epitaxial layer having the same conductivity type as the substrate. Makimoto, col. 3, lines 49-55. Electrical isolation is achieved by forming isolation channels having the same conductivity type as the regions formed in the substrate. Thus, the insulation technique used in the Makimoto reference is the same technique disclosed in applicant's Figure 1. In our opinion one having ordinary skill in the art would have recognized that Frouin's isolation technique is an alternative to the technique taught by Makimoto. It would have been obvious, therefore, to substitute Frouin's isolatin technique for Makimoto's technique. The motivations to use Frouin's technique comes from Frouin's teaching of the benefits of the oxide channel technique over the utilization of a material having the same conductivity type. Frouin, col. 2, lines 31-51. It would similarly be obvious for the reason already stated above to use a the single mask technique taught by Murphy to etch and oxidize the insolation channels and to substitute oxide alone for the combination of oxide and polycrystalline silicon as suggested from Doo's disclosure. The subject matter of claims 25 and 49 would have been prima facie obvious.

Applicant argues that the teachings of the Frouin, Murphy, Doo and Makimoto references are not combinable. We do not agree. All the references relate to a process for manufacturing integrated circuits having electrically isolated regions. They are clearly from the same field of endeavor and therefor constitute analogous prior art. In re Deminski, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986); In re Wood, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979), cert. denied, 111 S. Ct. 1682 (1991). The hypothetical person of ordinary skill in the art is thus charged with knowledge of the content of those references. In re Dillon, 919 F.2d 688, 694, 16 USPQ2d 1897, 1902 (Fed. Cir. 1990) (in banc). The teachings of analogous prior art references are combinable. In re Reuter, 670 F.2d 1015, 1020 n.7, 210 USPQ 249, 254 n.7 (CCPA 1981); In re Kyser, 588 F.2d 303, 307, 200 USPQ 211, 214 (CCPA 1978); In re Menough, 323 F.2d 1011, 1013, 139 USPQ 278, 280 (CCPA 1963). Thus, the teachings of Frouin, Murphy, Doo and Makimoto are combinable. In any event, one having ordinary skill in the art would have been motivated to utilize Murphy's channel forming technique and eliminate the polycrystalline semiconductor deposition and removal steps taught by Frouin. Additionally, the person having ordinary skill in the art would have known, from Doo's disclosure, that the combination of polycrystalline silicon and silicon oxide is an alternative to silicon oxide in forming electrical insulation channels. Doo, col. 5, lines 12-15. An express suggestion to substitute one alternative for another need not be present to render such substitution obvious. In re Fout, 675 F.2d 297, 301, 213 USPQ 532, 536 (CCPA 1982). Similarly, the person having ordinary skill in the art would have been motivated to substitute Frouin's technique for Makimoto's for the reasons already stated above.

Claims 2-3, 5, 6, 12, 15, 19, 20, 26-28, 30, 31, 33-35, 37-41, 48, 50-52 and 59

Applicant's brief does not assert the separate patentability of these claims over the claims from which they depend. Accordingly, claims 2-3, 5, 6, 12, 15, 19, 20, 26-28, 30, 33-35, 37-41, 48, 50-52 and 59 fall with their respective independent claims.

Claims 7-9, 29, 32, 42-47, and 53-58

Applicant asserts that these claims recite material that makes the claims patentable separate from the other claims. More particularly, applicant asserts claims 7, 29, 42 and 53 require a "multi-part semiconductor pocket" and the examiner has not proffered any evidence showing this feature to have been obvious. Brief, p. 20. The examiner responds indicating that Frouin, Figure 7, discloses a multi-part pocket.

We reverse the rejection of these claims.

We can not agree with the examiner that Frouin, Figure 7 renders obvious the additional required steps of claims 7, 29, 42 and 53 and the claims dependent therefrom. As pointed out by applicant (Brief p. 5-6), the subject matter of these claims require formation of a low resistivity buried layer which crosses under an oxide channel forming a pocket including two separate epitaxial areas connected by a single low resistivity area. Frouin's Figure 7 does not suggests the claimed steps for making such a pocket. Nor has the examiner presented a rationale as to why the steps would have otherwise been obvious.

The rejections based upon Doo, Jones, Clevenger, and Murphy.

Claims 2-3, 5-9, 12, 14, 15, 19, 20, and 36-48 stand rejected under 35 U.S.C. § 103 as unpatentable over the combination of Doo or Jones and Clevenger and Murphy. Claims 25-35 and 49-59 are rejected under 35 U.S.C. § 103 over these same references additionally combined with Karcher or Makimoto. We reverse these rejections.

In the examiner's view, Doo and Jones each teach a process of combining PN junction horizontal isolation with oxide side-wall isolation by growing an epitaxial layer through an oxide mask. The examiner considers Clevenger and Murphy as teaching that the selective growth of an epitaxial layer through an oxide mask and the sinking an oxide region into a single crystal layer by selective oxidation using a silicon nitride mask are alternative procedures. The examiner then concludes that it would have been "an obvious alternate and essentially equivalent process to form the oxide sidewalls in the Doo or Jones process by the sunken oxide technique of Clevenger or Murphy." Examiner's Answer, p. 7.

The examiner has failed to establish a prima facie case of unpatentability. The examiner has not made findings as to the differences between the Doo/Jones process and the claimed invention as required by Graham v. John Deere, 383 U.S. 1, 18 (1966). Additionally, assuming the examiner is correct about that the person having ordinary skill in the art would recognize that selective growth of an epitaxial layer through an oxide mask and the sinking an oxide region into a single crystal layer by selective oxidation using a silicon nitride mask are alternative procedures, we fail to see how this information would be used to modify the Doo/Jones fabrication process to result in a process falling within the scope of applicant's claims. Accordingly, we reverse the rejection of claims 2, 3, 5, 6-9, 12, 14, 15, 19, 20, 25-32, 36-59 based on the combination including Doo, Jones, Clevenger, and Murphy.

CONCLUSION

The rejection of claims 2, 3, 5, 6, 12, 14, 15, 19, 20, 25-28, 30, 31, 33-41, 48-52 and 59 under 35 U.S.C. § 103 is affirmed. The rejections of claims 7-9, 29, 30, 32, 42-47, and 53-58 are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

EDWARD C. KIMLIN Administrative Patent Judge	)	
RICHARD E. SCHAFER Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
CAMERON WEIFFENBACH Administrative Patent Judge	)	

bae

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